

WHAT IS CLAIMED IS:

1. A method for forming an opening, the method comprising:
providing a dielectric layer on a substrate;
forming a patterned photoresist layer on the dielectric layer, wherein at least a portion of the dielectric layer is exposed through the patterned photoresist layer;
etching the exposed portion of the dielectric layer;
performing a plasma treatment on the photoresist layer using a nitrogen-based gas; and
performing a wet strip to remove the patterned photoresist layer.
2. The method of claim 1 wherein the plasma treatment is selected to remove a by-product formed on the patterned photoresist layer during the etching.
3. The method of claim 1 wherein using a nitrogen-based gas includes using at least one of N₂, N₂/Ar, N₂/H₂, or NH₃.
4. The method of claim 1 wherein performing the wet strip includes using a wet resist stripping solution comprising at least one of DI/O₃, NH₄OH/DI/O₃, a sequence of SPM + APM, or a sequence of APM+SPM+APM, wherein DI is deionized water, APM is an ammonia peroxide mixture (NH₄OH and H₂O₂), and SPM is a sulphuric peroxide mixture (H₂SO₄ and H₂O₂).
5. A method for fabricating a borderless interconnection in a semiconductor device, wherein the device includes a photoresist layer defining a contact mask, an interlevel dielectric (ILD) layer, a stop layer, and a metal silicide layer, the method comprising:
etching the ILD layer to expose at least a portion of the stop layer, wherein the etching is guided by the contact mask;

performing a plasma treatment on the exposed portion of the stop layer;
removing at least the exposed portion of the stop layer to expose a portion of the metal silicide layer;
stripping the photoresist;
depositing a barrier layer over the exposed portion of the metal silicide layer; and
planarizing any layers above the ILD layer to expose the ILD layer.

6. The method of claim 5 wherein the barrier layer is deposited using a chemical vapor deposition process.

7. The method of claim 5 wherein the planarizing is accomplished using a chemical mechanical planarization process.

8. The method of claim 5 wherein a sputtering process is used in removing the exposed portion of the stop layer.

9. The method of claim 5 wherein a dry etch process is used in removing the exposed portion of the stop layer.

10. The method of claim 5 wherein performing the plasma treatment includes using at least one of N₂, N₂/Ar, N₂/H₂, or NH₃.

11. The method of claim 5 wherein stripping the photoresist includes using
a wet resist stripping solution comprising at least one of DI/O₃, NH₄OH/DI/O₃, a sequence of SPM + APM, or a sequence of APM+SPM+APM, wherein DI is deionized water, APM is an ammonia peroxide mixture (NH₄OH and H₂O₂), and SPM is a sulphuric peroxide mixture (H₂SO₄ and H₂O₂).

12. A method for fabricating an opening in a semiconductor device, wherein the device includes upper, middle, and lower layers, the method comprising:

removing at least a portion of the upper layer to expose a corresponding portion of the middle layer;

performing a plasma treatment on the exposed portion of the middle layer using a nitrogen-based plasma; and

removing the exposed portion of the middle layer using a wet strip process, wherein damage to the lower layer is minimized due to the plasma treatment.

13. The method of claim 12 wherein removing the upper layer includes using a dry etch process.

14. The method of claim 12 further comprising:

depositing a photoresist layer above the upper layer, wherein the photoresist layer defines a pattern that controls the removing of the upper layer; and

removing the photoresist layer using a wet stripping process.

15. The method of claim 14 wherein removing the middle layer includes using a dry etch process.

16. The method of claim 14 wherein removing the middle layer includes using a sputtering process.

17. The method of claim 12 further comprising depositing the upper, middle, and lower layers in a contiguous manner on a substrate.

18. A method for minimizing damage to a semiconductor device while creating an opening in the device, wherein the device includes an etch stop layer

that is contiguous with an underlying metal silicide layer, the method comprising:

applying a nitrogen plasma treatment to at least a portion of the etch stop layer; and

removing the treated portion of the etch stop layer to expose a portion of the underlying metal silicide layer, wherein the plasma treatment reduces damage to the underlying metal silicide layer that occurs during the removing of the treated portion of the etch stop layer.

19. The method of claim 18 wherein the etch stop layer is removed using a dry etch process.

20. The method of claim 18 wherein the etch stop layer is removed using an argon sputtering process.

21. The method of claim 18 wherein applying the nitrogen plasma treatment includes using at least one of N₂, N₂/Ar, N₂/H₂, or NH₃.

22. The method of claim 18 further comprising:
depositing the etch stop layer, wherein the etch stop layer comprises silicon nitride or silicon oxynitride; and
depositing the metal silicide layer, wherein the metal silicide layer comprises nickel silicide.

23. The method of claim 22 further comprising:
depositing an interlevel dielectric (ILD) layer above the etch stop layer;
depositing a photoresist layer above the ILD layer, wherein the photoresist layer defines a pattern that controls removing the ILD layer; and
removing the ILD layer according to pattern, wherein the removal of the ILD layer defines the portion of the etch stop layer to which the nitrogen plasma treatment is applied.

24. The method of claim 23 further comprising removing the photoresist layer using a wet stripping process.

25. The method of claim 23 further comprising degrading residual matter left after the ILD layer is removed, wherein the degrading is accomplished using the nitrogen plasma treatment.

26. The method of claim 23 further comprising:
depositing a barrier layer on the exposed portion of the metal silicide layer;
depositing a blanket metal layer on the barrier layer; and
planarizing a portion of the metal blanket layer to expose the ILD layer.